Designing with the UltraScale Architecture

Course Description
This course introduces new and experienced designers to the most sophisticated aspects of the UltraScale™ architecture. Targeted towards designers who have used the Vivado® Design Suite, this course focuses on designing for the new and enhanced resources found in our newest FPGA family. Topics covered include an introduction to the new CLB resources, the clock management resources (MMCM and PLL), global and regional clocking resources, memory and DSP resources, and source-synchronous resources. A description of the improvements to the dedicated transceivers and Transceiver Wizard is also included. Use of the Memory Interface Generator (MIG) and the new DDR4 memory interface capabilities is also covered. In addition, you will learn how to best migrate your design and IP to the UltraScale architecture and the best way to use the Vivado Design Suite during design migration. A combination of modules and labs allow for practical hands-on experience of the principles taught.

Level: FPGA 3
Training Duration: 2 days

Who Should Attend?
Anyone who would like to build a design for the UltraScale device family.

Prerequisites:
• Completion of the Essentials of FPGA Design course and Vivado Design Suite STA and Xilinx Design Constraints course
• OR completion of the Vivado Advanced XDC & STA for ISE Users course

Software Tools:
• Vivado™ Design or System Edition 2014.1

Hardware:
• Architecture: UltraScale FPGAs*
• Demo board: None*

Skills Gained: After completing this training, you will be able to:
• Take advantage of the primary UltraScale architecture resources
• Describe the new CLB capabilities and the impact that they make on your HDL coding style
• Define the block RAM, FIFO, and DSP resources available
• Properly design for the I/O and SERDES resources
• Identify the MMCM, PLL, and clock routing resources included
• Identify the hard IP resources available for implementing high-performance DDR4 memory interfaces
• Describe the additional features of the dedicated transceivers
• Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

Course Outline
1. UltraScale Architecture Overview
2. Design Migration Software Recommendations
3. CLB Architecture and HDL Coding Styles
4. Lab 1: Optimal Coding Styles for CLB Resources
5. Clocking Resources
6. Lab 2: Clocking Migration
7. Lab 3: Clocking Resources
8. Memory and DSP Resources
9. Lab 4: DDR3 MIG Design Migration
10. Lab 5: DDR4 MIG Design Creation
11. I/O Resources
12. FPGA Design Migration
13. Design Migration Case Study
14. Lab 6: QSGMII Design Migration
15. Lab 7: 10G PCS/PMA and MAC Design Migration
16. Transceiver Wizard Demonstration
17. Transceiver Overview
18. Lab 8: Transceiver Core Resources

Lab Description
Lab 1: Optimal Coding Styles for CLB Resources – Analyze a design that has asynchronous resets by generating various reports such as the Timing Summary report and Utilization report. Convert the asynchronous resets to synchronous resets by removing the reset signal from the sensitivity list. Also examine the CLB resources, such as the LUT and the dedicated carry chain.
Lab 2: Clocking Migration – Migrate a 7 series design to the UltraScale architecture with a focus on clocking resources.
Lab 3: Clocking Resources ndash; Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks.
Lab 4: DDR3 MIG Design Migration – Migrate a 7 series MIG design to the UltraScale architecture. The provided MIG design was targeted to a Kintex® UltraScale device (KC705 evaluation board) with DDR3 memory on board. In this case, the design will be migrated to use an UltraScale DDR3 memory interface.
Lab 5: DDR4 MIG Design Creation – Create a DDR4 memory controller with the Memory Interface Generator (MIG) utility.
Lab 6: QSGMII Design Migration – Migrate an existing 7 series QSGMII example design to a Kintex UltraScale architecture-based device. This lab will show you how to update your port connections and use the optimum logic resources available.
Lab 7: 10G PCS/PMA and MAC Design Migration – Migrate a successfully implemented 7 series design containing 10G Ethernet MAC and 10G PCS/PMA IP to an UltraScale FPGA.
Lab 8: Transceiver Core Resources – Use the Transceiver Wizard to build a design that uses a single serial transceiver and observe the file structures created.