Vivado Design Suite Advanced XDC and Static Timing Analysis for ISE Software Users

Course Description

This course will update experienced ISE software users to utilize the Vivado Design Suite. Learn the underlying database and static timing analysis (STA) mechanisms. Utilize Tcl for navigating the design, creating Xilinx design constraints (XDC), and creating timing reports. Learn to make appropriate timing constraints for SDR, DDR, source-synchronous, and system-synchronous interfaces for your FPGA design.

You will also learn to make path-specific, false path, and min/max timing constraints, as well as learn about timing constraint priority in the Vivado timing engine. Finally, you will learn about the scripting environment of the Vivado Design Suite and how to use the project-based scripting flow.

You will also learn the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level: FPGA 2

Training Duration: 2 days

Who Should Attend?

Existing Xilinx ISE® Design Suite FPGA designers

Prerequisites:

- Completion of the Vivado Design Suite for ISE Project Navigator Users course is strongly recommended.
- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Software Tools:

Vivado® System Edition 2017.3

Hardware:

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: None*

Skills Gained: After completing this training, you will be able to:

- Create appropriate clock and input, output delay constraints and describe timing reports that involve input and output paths
- Analyze different timing reports
- Define a properly constrained design
- Describe setup and hold checks and describe the components of a timing report
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Describe all of the options available with the report_timing and report_timing_summary commands
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Describe the timing constraints required to constrain system-synchronous and source-synchronous interfaces
- Identify timing closure techniques using the Vivado® Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experiences

Course Outline

1. Introduction to Clock Constraints

2. Generated Clocks

Use the report clock networks report to determine if there are any generated clocks in a design.

3. Report Clock Networks

Use report clock networks to view the primary and generated clocks in a design.

4. Clock Group Constraints

Apply clock group constraints for asynchronous clock domains.

5. I/O Constraints and Virtual Clocks

6. Timing Constraints Wizard

7. Introduction to Vivado Reports

Generate and use Vivado timing reports to analyze failed timing paths.

8. Setup and Hold Timing Analysis

Understand setup and hold timing analysis.

Lab Description

1. Introduction to Clock Constraints

Apply clock constraints and perform timing analysis.

2. I/O Constraints and Virtual Clocks

Apply I/O constraints and perform timing analysis.

3. Timing Constraints Wizard

Use the Timing Constraints Wizard to apply missing timing constraints in a design.

4. Introduction to Timing Exceptions

Introduces timing exception constraints and applying them to fine tune design timing.

5. Synchronization Circuits

Use synchronization circuits for clock domain crossings.

6. Baselining

Use Xilinx-recommended baselining procedures to progressively meet timing closure.

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Cont...

9. Timing Summary Report

Use the post-implementation timing summary report to sign-off criteria for timing closure.

10. Report Clock Interaction

Use the clock interaction report to identify interactions between clock domains.

11. Introduction to Timing Exceptions

12. Timing Constraints Priority

Identify the priority of timing constraints.

13. Synchronization Circuits

14. Report Datasheet

Use the datasheet report to find the optimal setup and hold margin for an I/O interface.

15. UltraFast Design Methodology: Implementation

Introduces the methodology guidelines covered in this course.

16. Baselining

17. Pipelining

18. I/O Timing Scenarios

Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.

19. System-Synchronous I/O Timing

Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.

20. Source-Synchronous I/O Timing

21. Introduction to Floorplanning

Introduction to floor planning and how to use Pblocks while floor planning.

22. Congestion

Identifies congestion and addresses congestion issues.

23. Physical Optimization

24. UltraFast Design Methodology: Design Closure

Introduces the design methodology guidelines covered in this course.

7. Pipelining

Use pipelining to improve design performance.

8. Source-Synchronous I/O Timing

Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.

9. Physical Optimization

Use physical optimization techniques for timing closure.