AXI3 / AXI4 INTERCONNECT

Duration: 2 Days

Related courses:
AXI v4 is the interconnect used by Cortex-A and Cortex-R ARM CPUs, see the outlines of these courses

Course objectives:
- This course details first the AXI3 protocol
- New signals present in AXI4 are then described
- The course explains the AXI4 stream protocol and indicates in which case this simplified protocol is suitable
- AXI4-lite protocol is described
- The NIC-301 interconnect IP is studied, clarifying synthesis options as well as software QOS parameterizing
- AXI Coherency Extensions (ACE) new channels are explained through an overall introduction to snooping
- The CCI-400 interconnect IP is described, highlighting the purpose of ACE-lite ports

Prerequisites:
- Knowledge of an interconnect, such as IBM CoreConnect or ARM AHB is recommended

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Course Content:

First day

1. AXI3 PROTOCOL [4-hour]
- ARM AMBA versions
- Address and data channels
- Basic read and write transactions, pipelining, data reordering
- Global signals, clocking, low power handshake interface
- Detailing address channel signals
  - Clarifying cache related signals, allocate policies
  - Explaining bufferable vs not bufferable attribute
- Detailing data channel signals
  - Using write strobe signals, managing unaligned transfers
- Detailing response signals
- Ordering model, composite transaction ID
- Managing exclusive resources, local and global monitors
- AXI Master parameter list
- AXI Slave parameter list

2. AXI4 NEW SIGNALS [1/2-hour]
- AXI4 slave response dependencies
- QoS signalling, defining a per-transaction priority
- Multiple region signalling
- User signals, implementation example in Cortex-A9

3. AXI4 LITE [1/2-hour]
- Simpler control register-style interface
- Bursts of 1 data beat
- Signal list, highlighting the AXI4 non supported signals
- Conversion, protection and detection

4. AXI4 STREAM [1-hour]
- Objectives of this new protocol
- Byte definition: data byte, null byte, position byte
- Byte stream example
- Signal list
- Merging and packing
- Downsizing / upsizing
- Packet transfer
- Source and destination signaling

5. NIC-301 AXI3 INTERCONNECT [2-hour]
- Block diagram
- Bus conversion wrappers
- TrustZone support
- Programmable features, QoS
- Arbitration algorithms: Round Robin, Least Recently Granted
- Slave and master interface options
- Programmer's model

Second day

6. INTRODUCTION TO CACHE AND TLB COHERENCY [2-hour]
- Cache organization
- Explaining the need for coherency
- Software coherency
- Hardware coherency
- Translation Lookaside Buffer
- Implementing an I/O MMU

Continued …

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7. AXI COHERENCY EXTENSION [3-hour]
- Signals added to the traditional 5 channels
- Explaining what is a shareability domain
- Using barriers, related ARM instructions
- The three additional channels
- ACE new transactions: explaining through sequences their utilization
  - Non-cached transactions
  - Shareable read transactions
  - Shareable write transactions
  - Write-back transactions
  - Cache maintenance transactions
- Distributed virtual memory
- ACE-lite subset

8. CCI-400 AXI4 ACE INTERCONNECT [2-hour]
- SoC architecture example
- CCI-400 features, implementation in a Big/little system
- Speculative fetch
- Performance monitoring unit
- TrustZone support
- Error responses
- QoS value arbitration and propagation
- Regulation of outstanding transactions
- QoS value based on latency measurement

9. Summary