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Authorized Training Provider
XILINX®

Advanced FPGA Implementation

Course Description

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE® design suite and Xilinx hardware. Labs provide hands-on experience in this two-day training and cover the Xilinx Synthesis Technology (XST) tools.
This course requires the Essentials of FPGA Design and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE tools and 7 series FPGAs.

Level: FPGA 4

Training Duration: 2 days

Who Should Attend?

Engineers who seek advanced FPGA design training using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites:

- Essentials of FPGA Design
- Designing for Performance
- Intermediate knowledge of VHDL or Verilog is strongly recommended
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools:

- Xilinx ISE Design Suite: Logic or System Edition 14.7

Hardware:

- Architecture: 7 series FPGAs*

Skills Gained: After completing this training, you will be able to:

- Create and edit a User Constraint File (UCF)
- Identify the I/O timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Implement designs via the Tcl command line
- Use the PlanAhead™ tool to create area constraints
- Use design preservation techniques to simplify design ripple effects
- Change signals of interest in the ChipScope™ Pro tool for board-level debugging using the FPGA Editor

Course Outline

Introduction

Lab 1: Timing Closure Review

UCF Editing

Lab 2: UCF Editing

Advanced I/O Timing

Lab 3: Advanced I/O Timing

Tcl Scripting

Lab 4: Tcl Scripting

Floorplanning an Effective Layout

Lab 5: Floorplanning

Design Preservation Techniques

FPGA Editor: Viewing and Editing a Routed Design

Lab 6: Advanced FPGA Editor

Lab Description

Lab 1: Timing Closure Review – Use the Constraints Editor to enter timing constraints.
Lab 2: UCF Editing – Write constraints directly into a UCF file to guide the performance results of implementation.
Lab 3: Advanced I/O Timing – Compose timing constraints for source-synchronous and system-synchronous I/O interfaces. Analyze the timing and determine changes to optimize the interface timing.
Lab 4: Tcl Scripting – Write ISE tool control commands in Tcl script files to create a project and implement the design. Explore how the Tcl interface is integrated with the Project Navigator tool.
Lab 5: Floorplanning – Implement a design by using floorplanned constraints to improve the timing results over a design without floorplanning.
Lab 6: FPGA Editor – Use the FPGA Editor to view and edit a design. Rapidly locate and swap signals of interest for ChipScope Pro tool cores.