CYCLONE-V CORTEX-A9 HARD PROCESSOR SYSTEM

Training Duration: 5 days

Prerequisites:
- Knowledge of ARM7/9.
- This course does not include chapters on low level programming.
- Experience of processor integrated in FPGA, such as PowerPC or NIOS is recommended.

Related courses:
- Programming with RVDS IDE (http://www.ac6-formation.com/cours.php/catID_20/coursID_186.xphp)
- VFP programming (http://www.ac6-formation.com/cours.php/catID_20/coursID_185.xphp)
- NEON programming (http://www.ac6-formation.com/cours.php/catID_/coursID_159.xphp)
- Ethernet (http://www.ac6-formation.com/cours.php/catID_23/ref_N1.xphp)
- USB 2.0 (http://www.ac6-formation.com/cours.php/catID_21/ref_IP2.xphp)
- CAN bus (http://www.ac6-formation.com/cours.php/catID_21/ref_IA1.xphp)

Practical labs:
- Labs are run under RVDS 4.1

Course objectives:
- This course aims to clarify the Cyclone-V Cortex-A9 Hard Processor System
- The interconnect based on ARM NIC-301 is particularly detailed
- Hardware implementation of the Cortex-A9 is described, including reset and clocking
- The possible boot sequences, involving or not the FPGA configuration, are explained
- Interaction between level 1 caches, level 2 cache and main memory is studied through sequences
- MMU operation is described
- Spin-lock implementation in a multicore system is also detailed
- The exception mechanism is explained, focusing on Cyclone-V interrupt mapping
- An overview of the Coresight specification is provided prior to describing the debug related units and general Cyclone-V debug infrastructure, involving both the Hard Processor System and the FPGA portion
- The operation of the Snoop Control Unit when supporting SMP is fully explained, particularly the utilization of cache tag mirrors, the advantage of connecting DMA channels to ACP and the sequences that have to be used to modify a page descriptor
- Integrated SDRAM and Flash controllers, which can be accessed by FPGA masters and processor block masters, are fully described
- Integrated peripherals are studied, especially the gigabit Ethernet MACs and the USB2.0 OTG controllers

Documentation
Training manuals will be given to attendees during training. Precise and easy to use, those notes can be used as a reference afterwards.

Course Content:

First day
INTRODUCTION TO CORTEX-A9 [1-hour]
- Block diagram, 1 or 2 AXI master interfaces
- Cortex-A9 variants: single core vs multicore
- New memory-mapped registers in MPCore
- The 3 instruction sets
- Instantiated options: cache size, Jazelle, NEON, FPU, PTM and IEM

CYCLONE-V OVERVIEW [1-hour]
- Hard Processor System block diagram
- FPGA portion
- On-chip memories
- Possible boot scenario
- HPS-FPGA interfaces
- Address mappings, translation when implementing ACP

CLOCK AND RESET MANAGERS [1-hour]
- Reset sources
- Hardware sequenced resets
- Block diagram, integrated three PLLs
- Clock usage by module
- Main clock group
- Cortex-A9 clock scaling
- Software managed clocks

BOOTING AND CONFIGURATION [1-hour]
- Boot sequence
- Selecting the interface from which the boot code will be loaded
- Indirect vs direct code execution
- Initial software, boot loader
- Initial software image layout
- Independent HPS booting and FPGA configuration

AMBA 4 [2-hour]
- AXI
  - Topology: direct connection, multi-master, multi-layer
  - Separate address/control and data phases
  - AXI channels, channel handshake
  - Support for unaligned data transfers

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Course Content:

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- Transaction ordering, out of order transaction completion
- Read and write burst timing diagrams
- Cortex-A9 external memory interface, ID encoding
- NIC-301 AXI interconnect
- APB 3

MEMORY MANAGEMENT UNIT [2-hour]
- MMU objectives
- Page sizes
- Address translation
- Page access permission, domain and page protection
- Page attributes, memory types
- Utilization of memory barrier instructions
- Format of the external page descriptor table
- Tablewalk
- TLB organization
- TLB lockdown
- Utilization of microTLBs
- Abort exception, on-demand page mechanism
- MMU maintenance operations
- Using a common page descriptor table in an SMP platform, maintaining coherency of multiple TLBs
- PMU related events
- Related CP15 registers

Second day
LEVEL 1 MEMORY SYSTEM [2-hour]
- Cache organization
  - Virtual indexing, physical tagging for instruction cache ; physical indexing and tagging for data cache
  - Supported maintenance operations
  - Write-back write allocate cache allocation
  - Memory hint instructions PLD, PLI, PLDW, data prefetching
  - Describing transient cache related transactions: line fills and line eviction
  - No lockdown support
  - 4-entry 64-bit merging store buffer
  - PMU related events

HARDWARE COHERENCY [2-hour]
- Snooping basics: CLEAN, CLEAN & INVALIDATE and INVALIDATE snoop requests
- Snoop Control Unit: cache-to-cache transfers
- MOESI state machine
- Address filtering
- Understanding through sequences how data coherency is maintained between L2 memory and L1 caches
- Accelerator Coherency Port: connecting a DMA channel that uses this port to enforce coherency of data it is transmitting

- Enabling coherency mode
PL310 LEVEL 2 CACHE [2-hour]
- Cache configurability
- AXI interface characteristics
- Exclusive mode operation when connected to Cortex-A9
- Understanding through sequences how cacheable information is copied from memory to level 1 and level 2 caches
- Transient operations, utilization of line buffers LFBs, LRBs, EBs and STBs
- Discarding a level 3 memory line load through merging writes into STBs
- TrustZone support
- Power management
- Cache event monitoring
- Memory mapped registers included in the cache controller
- Describing each maintenance operation
- Cache lockdown, implementation of a small memory by a boot program
- Initialization sequence
- Interrupt management

SYSTEM INTERCONNECT [2-hour]
- Interconnect block diagram, master-to-slave connectivity matrix
- Bridge to APB, L4 slaves
- L3 main switch
- QoS, arbitration policies
- Cyclic dependencies avoidance schemes
- Address remapping
- ACP ID mapper
- HPS-to-FPGA AXI bridge
- FPGA-to-HPS AXI bridge, directly accessing SDRAM from FPGA masters with or without hardware cache coherency
- Clarifying the conditions for an FPGA IP to use hardware coherency

Third day
MEMORY CONTROLLERS [3-hour]
- On Chip RAM
  - ECC support
- Integrated DDR3 controller
  - Introduction to DDR3, write levelling, ZQ calibration, reset
  - ECC control
  - Parameterizing the controller according to DDR3 device timings
  - FPGA-to-HPS SDRAM port utilization, 64-, 128- or 256-bit Avalon or AXI ports
  - Multiport scheduling
  - AXI global monitor
  - Command reordering
- NAND flash controller
  - Discovery and initialization

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Course Content:

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- Data DMA
- ECC control
- SD/MMC controller
  - Card detection and initialization
  - Booting from SD/MMC
  - Integrated descriptor-based DMA
  - 4-KB data FIFO
  - Error management
- Quad SPI flash controller
  - Direct access and indirect access modes
  - Using a memory-mapped interface to automatically initiate flash page reads / writes
  - XIP flash device
  - Local memory buffer
  - STIG operation

CORTEX-A9 HARDWARE IMPLEMENTATION [2-hour]
- Clock domains
- Reset domains, power-on reset, debug and Data Engine logic reset
- Power control, dynamic power management
- Wait For Interrupt architecture
- AXI master interface attributes
- Level 2 memory interface: AXI read & write issuing capability
- Exclusive L2 cache
- AXI sideband information

INTERRUPT CONTROLLER [2-hour]
- Cortex-A9 exception management: enforcing a particular endian mode on exception entry, configuring FIQ to be non maskable, configuring the default exception handling state: ARM vs Thumb
- Cyclone-V interrupt mapping
- Interrupt virtualization
- Integrated timer and watchdog unit in MPCore
- Interrupt groups: STI, PPI, SPI, LSPI
- Legacy mode: direct IRQ and FIQ
- Assigning a security level to each interrupt source (Secure or Non Secure)
- Prioritization of the interrupt sources

Fourth day
CORESIGHT DEBUG UNITS [3-hour]
- Benefits of CoreSight
- Invasive debug, non-invasive debug, taking into account the secure attribute
- APBv3 debug interface
- Connection to the Debug Access Port
- Debug facilities offered by Cortex-A9
- Process related breakpoint and watchpoint
- Program counter sampling
- Event catching

- Debug Communication Channel
- PTM interface, connection to funnel
- Debugging while the processor is in shutdown or dormant mode
- Debug registers description
- Miscellaneous debug signals
- Cross-Trigger Interface, debugging a multi-core SoC
- Generating debug events from / to the FPGA fabric
- Cyclone-V debug infrastructure
- System Trace Macrocell, generating trace information from FPGA fabric
- Embedded Trace FIFO
- Embedded Trace Router, routing trace data to a RAM which could be the on-chip RAM as well as the SDRAM
- SCAN manager:
  - Configuring and managing the HPS I/O pins
  - Communicating with the FPGA JTAG TAP
  - ARM JTAG Access Port

GPIO [1/2-hour]
- Pin direction configuration
- Digital debounce
- Configurable interrupt mode

FPGA MANAGER [1-hour]
- Managing and monitoring the FPGA portion
- Implementing 32 general purpose inputs and outputs from/to FPGA portion
- Handshaking inputs when booting from FPGA
- Generating interrupts based on changes in the FPGA portion
- Resetting the FPGA portion
- FPGA configuration, partial reconfiguration, MSEL pins

SYSTEM MANAGER [1-hour]
- Selecting EMAC PHY interfaces
- Selecting SD/MMC controller clock options
- Connecting CAN controllers to DMA channels
- Managing parity errors detected in HPS, injecting errors
- Providing the boot ROM code with boot information required to support HPS boot
- Selecting NAND flash controller boot options
- Configuring the USB controller

DMA CONTROLLER [2-hour]
- Memory-to-memory, memory-to-peripheral and peripheral-to-memory transfers
- 8 logical channels, arbitration
- Scatter / gather, list of descriptors
- 31 peripheral handshake interfaces
- DMA instruction execution engine, variable-length instructions, instruction set description
- Multi-FIFO operation
- Dual APB control interfaces to support Secure and NS operation
- Interrupt management

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- Operating states
- Using an event to restart a DMA channel
- Aborting a transfer

Fifth day
ETHERNET MACS [3-hour]
- Ethernet basics
- PHY connection, PHY management interface
- Buffer management, based on Buffer Descriptors
- Incoming frame filtering mechanisms, hash tables
- Flow control in full duplex mode
- VLAN support
- TCP-IP offload
- Audio video (AV) feature, transmitting time-sensitive informations
- IEEE1588 protocol support, timestamp registers
- Media Information Base

USB 2.0 OTG CONTROLLER [1-hour]
- Connecting the PHY
- Explaining what is OTG, SRP and HNP
- The 2 USB ports
- High-speed operation
- Host operation, muxing periodic and non-periodic traffics
- Low power modes
- Endpoint configuration

LOW SPEED SERIAL INTERFACES [2-hour]
- Synchronous Serial Port
  - SPI, Microwire, or TI synchronous serial interface
  - SPI protocol basics
  - Master / slave operation
  - External chip-select
  - FIFO mode, DMA support
- I2C interfaces
  - I2C protocol basics
  - High-Speed mode
  - Master vs slave
  - Multimaster operation
  - Transfer sequence
  - DMA support
- UART
  - 16550 / 16750 compatibility
  - Modem control signals, hardware flow control
  - FIFO mode, connection to DMA channels
  - Interrupt FIFO Level Select
  - Line break generation and detection

- CAN
  - Message objects:128 message buffers
  - Acceptance filtering
  - External DMA interface
  - Automatic retransmission
  - Test mode

HPS CORE INSTANTIATION [1-hour]
- Configuring FPGA interfaces
- Configuring peripheral pin muxing
- Configuring HPS clocks
- Configuring the external memory interface
- Address span extender component
- Generating the HPS core