

DSP Design Using System Generator

Course Description

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

Level: DSP 3

Training Duration: 2 days

Who Should Attend?

System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design.

Prerequisites:

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Software Tools:

- Vivado® System Edition 2016.3
- MATLAB with Simulink software R2016b

Hardware:

- Architecture: 7 series and UltraScale™ FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board or Kintex UltraScale™ FPGA KCU105 board and Zynq®-7000 All Programmable SoC ZC702 or ZedBoard*

Skills Gained: After completing this training, you will be able to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Run hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Implement multi-rate systems in System Generator
- Integrate System Generator models into the Vivado IDE
- Design a processor-controllable interface using System Generator for DSP
- Generate IPs from C-based design sources for use in the System Generator environment

Course Outline

1. Introduction to System Generator
2. Simulink Software Basics
3. Basic Xilinx Design Capture
4. Signal Routing
5. Implementing System Control
6. Multi-Rate Systems
7. Filter Design
8. System Generator, Vivado Design Suite, and Vivado HLS Integration
9. Kintex-7 FPGA DSP Platforms

Lab Description

Lab 1: Using the Simulink Software

Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.

Demo: System Generator Gateway Blocks

Lab 2: Getting Started with Xilinx System Generator

Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.

Lab 3: Signal Routing

Design padding and unpadding logic by using signal routing blocks.

Lab 4: Implementing System Control

Design an address generator circuit by using blocks and Mcode.

Lab 5: Designing a MAC-Based FIR

Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.

Lab 6: Designing a FIR Filter Using the FIR Compiler Block

Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.

Lab 7: System Generator and Vivado IDE Integration

Embed System Generator models into the Vivado IDE.

Lab 8: System Generator and Vivado HLS Tool Integration

Generate IP from a C-based design to use with System Generator.

Lab 9: AXI4-Lite Interface Synthesis

Package a System Generator for DSP design with an AXI4-Lite interface and integrate this packaged IP into a Zynq All Programmable SoC processor system.