Debugging Techniques using the ChipScope Protool

Course Description

As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use ChipScope™ Pro tool solution helps minimize the amount of time required for verification and debug.

This two-day course will not only introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug logic and high-speed designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address advanced verification and debugging challenges.

Level: FPGA 2

Training Duration: 2 days

Who Should Attend?

System and logic designers who want to minimize verification and debug time.

Prerequisites:

- Basic language concepts for both days
- Designing with VHDL or equivalent knowledge of VHDL
- Designing with Verilog or equivalent knowledge of Verilog
- Basic FPGA skills for Day 1
- Essentials of FPGA Design
- Intermediate FPGA skills for Day 1
- Designing for Performance
- ChipScope Pro Software Overview Video strongly recommended

Software Tools:

- Xilinx ISE Design Suite: System Edition 13.1
- ChipScope Pro software 13.1

Hardware:

- Demo board: Spartan-6 FPGA SP605 board

Skills Gained: After completing this training, you will be able to:

- Identify each ChipScope Pro tool core and explain its purpose
- Effectively utilize the ChipScope Pro Analyzer tool
- Implement the ChipScope Pro tool using the CORE Generator™, Core Inserter, and PlanAhead™ tool flows
- Select effective test points in your design
- Optimize design and core performance when ChipScope Pro tool cores are used
- Execute various techniques for collecting data, including file storage, scripting, and building custom triggers

Course Outline

1. How the ChipScope Pro Tool Works

2. Inserting the Cores – Inserter Flows: Core Inserter and the PlanAhead Software

Labs 1 and 2: Using the Inserter Tool from Project Navigator and Using the Inserter Tool from the PlanAhead software

3. Instantiating the Cores – The CORE Generator Tool Flow
Lab 3: Using the CORE Generator Tool from Project Navigator

4. Triggering and Storage

5. Visualizing Data – The ChipScope Pro Analyzer Tool

Lab 4: Triggering and Visualization in the Analyzer Tool Tips and Tricks

Lab 5: Tips and Tricks

6. Time for Timing

7. Video Demo – Area Groups for Isolation

8. Case Studies

Lab 6: FPGA Editor Support for the ChipScope Pro Tool

9. Scripting (Optional)*

Lab 7: VIO Tcl Scripting (Optional)*

10. Remote Access (Optional)*

Lab 8: Remote Access (Optional)*

Lab Descriptions

Labs 1 and 2: Using the Inserter Tool from Project Navigator (Lab 1) and Using the Inserter Tool from the PlanAhead Software (Lab 2) – Insert an ICON and ILA cores into an existing netlist and debug a common problem.
Lab 3: Using the CORE Generator Tool from Project Navigator, – Build upon a provided design to create and instantiate a VIO core and observe its behavior using the ChipScope Pro Analyzer tool.
Lab 4: Triggering and Visualization in the Analyzer Tool – Configure triggers and view captured data using the ChipScope Pro Analyzer tool.
Lab 5: Tips and Tricks – Keep time across multiple sample windows; sample across multiple time domains; and implement a complex custom (unconventional) trigger.
Lab 6: FPGA Editor Support for the ChipScope Pro Tool – Change the signals being sampled by an ILA without having to reimplement the design.
Lab 7: VIO Tcl Scripting – Configure automated analysis.
Lab 8: Remote Access – Use the ChipScope Pro Analyzer tool to configure an FPGA, set up triggering, and view the sampled data from a remote location.