Designing FPGAs Using the Vivado Design Suite 4

Course Description

This course tackles the most sophisticated aspects of the Vivado® Design Suite and Xilinx hardware. This course enables you to use the advanced capabilities of the Vivado Design Suite to achieve design closure.

Level: FPGA 4

Training Duration: 2 days

Who Should Attend?

Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Prerequisites:

- Designing FPGAs Using the Vivado Design Suite 2 course
- Designing FPGAs Using the Vivado Design Suite 3 course
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools:

- Vivado System Edition 2017.3

Hardware:

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board*

* This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

Skills Gained: After completing this training, you will be able to:

- Apply appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Utilize floorplanning techniques to improve design performance
- Employ advanced implementation options, such as incremental compile flow, physical optimization techniques, and re-entrant mode as last mile strategies
- Utilize Xilinx security features, bitstream encryption, and authentication using AES for design and IP security
- Identify advanced FPGA configurations, such as daisy chains and gangs, for configuring multiple FPGAs in a design
- Debug a design at the device startup phase to debug issues related to startup events, such as MMCM lock and design coming out of reset
- Use Tcl scripting in non-project batch flows to synthesize, implement, and generate custom timing reports

Course Outline

1. UltraFast Design Methodology: Design Closure

Introduces the UltraFast™ methodology guidelines covered in this course.

2. Scripting in Vivado Design Suite Non-Project Mode

3. Hierarchical Design

Overview of the hierarchical design flows in the Vivado Design Suite.

4. Managing Remote IP

5. I/O Timing Scenarios

Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.

6. System-Synchronous I/O Timing

Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.

7. Source-Synchronous I/O Timing

8. Timing Constraints Priority

Identify the priority of timing constraints.

9. Case Analysis

Understand how to analyze timing when using multiplexed clocks in a design.

10. Introduction to Floorplanning

Introduction to floorplanning and how to use Pblocks while floorplanning.

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Lab Description

1. Scripting in Vivado Design Suite Non-Project Mode

Write Tcl commands in the non-project batch flow for a design.

2. Managing Remote IP

Store IP and related files remote to the current working project directory.

3. Source-Synchronous I/O Timing

Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.

4. Design Analysis and Floorplanning

Explore the pre- and post-implementation design analysis features of the Vivado IDE.

5. Incremental Compile Flow

Utilize the incremental compile flow when making last-minute RTL changes.

6. Physical Optimization

Use physical optimization techniques for timing closure.

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Course Outline
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11. Design Analysis and Floorplanning

12. Congestion

Identifies congestion and addresses congestion issues.

13. Introduction to the Xilinx Tcl Store

Introduces the Xilinx Tcl Store.

14. Incremental Compile Flow

15. Physical Optimization

16. Vivado Design Suite ECO Flow

17. Power Management Techniques

Identify techniques used for low power design.

18. Daisy Chains and Gangs in Configuration

Introduces advanced configuration schemes for multiple FPGAs.

19. Bitstream Security

Understand the Xilinx bitstream security features such as readback disable, bitstream encryption, and authentication.

20. Vivado Design Suite Debug Methodology

Employ the debug methodology for debugging a design using the Vivado logic analyzer.

21. Trigger and Debug at Device Startup

Debug the events around the device startup.

22. Trigger Using the Trigger State Machine in the Vivado Logic Analyzer

23. Debugging the Design Using Tcl Commands

24. Using Procedures in Tcl Scripting

Employ procedures in Tcl scripting.

25. Using Lists in Tcl ScriptingEmploy lists in Tcl scripting.

26. Using regexp in Tcl Scripting

27. Debugging and Error Handling in Tcl Scripting

Understand how to debug errors in a Tcl script.

7. Vivado Design Suite ECO Flow

Use ECO flow to make changes to a previously implemented design and apply changes to the original design.

8. Trigger Using the Trigger State Machine in the Vivado Logic Analyzer

Use trigger state machine code to trigger the ILA and capture data in the Vivado logic analyzer.

9. Debugging the Design Using Tcl Commands

Use Tcl scripting for VLA designs for adding probes and making connections to probes.

10. Using regexp in Tcl Scripting

Use regular expressions to find a pattern in a text file while scripting an action in the Vivado Design Suite.