Designing an Integrated PCI Express System

Course Description

Attending this course will provide students a working knowledge of how to implement a Xilinx PCI Express core in custom applications. This course offers students hands-on experience with implementing a Xilinx PCI Express system within the customer education reference design. With this experience, users can improve their time to market with the PCIe core design. Various Xilinx PCI Express core products will be enumerated to aid in selecting the proper solution. This course focuses on the AXI streaming interconnect.

Level: Connectivity 3

Training Duration: 2 days

Who Should Attend?

- Hardware designers who want to create applications using Xilinx IP cores for PCI Express® specification
- Software engineers who want to understand the deeper workings of the Xilinx PCI Express solution
- System architects who want to leverage key Xilinx advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites:

- Experience with PCIe specification protocol
- Knowledge of VHDL or Verilog
- Some experience with Xilinx implementation tools
- Some experience with a simulation tool, preferably the Vivado® simulator
- Moderate digital design experience

Software Tools:

- Vivado Design or System Edition 2017.1

Hardware:

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 board*

Skills Gained: After completing this training, you will be able to:

- Construct a basic PCIe system by:
  - Selecting the appropriate core for your application
  - Specifying requirements of an endpoint application
  - Connecting this endpoint with the core
  - Utilizing FPGA resources to support the core
  - Simulating the design
- Identify the advanced capabilities of the PCIe specification protocol and feature set

Course Outline

1. Course Introduction
2. Xilinx PCI Express Solutions
3. Connecting Logic to the Core – AXI Interface
4. PCIe Core Customization
5. Packet Formatting Details
6. Simulating a PCIe System Design
7. Endpoint Application Considerations
8. PCI Express in Embedded Systems
9. Application Focus: DMA
10. Design Implementation and PCIe Configuration
11. Root Port Applications
12. Debugging and Compliance
13. Interrupts and Error Management
14. Course Summary

Lab Description

Lab 0: Packaet Coding
This lab helps you recall basic PCI Express transaction layer packet formats.

Lab 1: Constructing the PCIe Core
This lab familiarizes you with the necessary flow for generating a Xilinx Integrated PCI Express Endpoint core from the IP catalog. You will select appropriate parameters and create the PCIe core used throughout the labs.

Lab 2: Simulating the PCIe Core
This lab demonstrates the timing and behavior of a typical link negotiation using the Vivado simulator. You will observe and capture transaction layer packets.

Lab 3: Using the PCI Express Core in IP Integrator
This lab familiarizes you with all the necessary steps and recommended settings to use the PCIe solutions in an IP integrator block design.

Lab 4: Implementing the PCIe Design
This lab familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream by using the Tandem configuration mode.

Lab 5: Debugging the PCIe Design
This lab illustrates how to use the Vivado logic analyzer to monitor the behavior of the core and a small endpoint application for proper operation.