Designing with Ethernet MAC Controllers

Course Description

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements. Become familiar with Ethernet IP core design architectures, core IP port naming conventions, and signal waveforms.

Level: Connectivity 3

Training Duration: 2 days

Who Should Attend?

Engineers who would like to come up to speed on utilizing Xilinx Ethernet connectivity solutions

Prerequisites:

- FPGA Design Experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx Vivado® software implementation tools
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools:

- Vivado Design or System Edition 2014.3

Hardware:

- Architecture: 7 series and UltraScale™ FPGAs*
- Demo board: Kintex®-7 KC705 board (optional)*

Skills Gained: After completing this training, you will be able to:

- Describe the basics of Ethernet standard, protocol, and OSI model
- Identify the various solutions that Xilinx offers for Ethernet connectivity
- Utilize various Ethernet cores either in a standalone mode or as a peripheral in a processor-based design
- Determine an appropriate core to use
- Develop software to drive the core and achieve desired functionality
- Integrate hard and soft IP into the EDK

Course Outline

Lab Description

Lab 1: Exploring Ethernet Frames – Perform a functional simulation of the Tri-Mode Ethernet MAC LogiCORE™ IP. This IP is available through the Vivado IP catalog tool. A Vivado Design Suite project, based on the Tri-Mode Ethernet MAC example design, is provided and includes a simulation testbench. You will use the Vivado simulator to analyze Ethernet frames and identify the components of the frames. You will then modify the testbench to view its effect on core behavior.

Lab 2: Advanced Ethernet Frames – Perform a functional simulation of a Vivado Design Suite project, based on the Tri-Mode Ethernet MAC example design, that is provided with several simulation testbenches. You will use these testbenches to generate various kinds of frames and observe how the core behaves to these received frames. AXI MAC register configuration commands will be modified to affect the behavior of the MAC core. You will also study various signals involved in identifying frames and classify them into good frames or bad frames.

Lab 3: AXI Ethernet Example Design – Create a new Vivado Design Suite project, use the IP catalog tool to generate an AXI Ethernet Subsystem core, and open the Xilinx-provided example design. You will then analyze, simulate, synthesize, and implement the design for the Kintex-7 FPGA.

Lab 4: Processor-Based Ethernet Design – Use the Vivado IP integrator tool to create an Ethernet-based embedded system. The design will be based around the MicroBlaze™ processor and the Ethernet Lite controller. The SDK tool will be used to create and build the lwIP Echo Server example software application. This lab encompasses the entire design experience from cradle to grave.

Lab 5: Analyzing 10GE MAC Frames – Investigate the PHY and client interfaces of the 10-Gigabit Ethernet MAC LogiCORE IP, available in the Vivado IP catalog, by performing a functional simulation. You will use the Vivado simulator to view these waveform signals.