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Authorized Training Provider
XILINX®

Designing with the Xilinx 7 Series

Course Description

Are you interested in learning how to effectively utilize 7 series architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the Essentials of FPGA Design course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family.
Topics covered include device overviews, CLB construction, MMCM and PLL clocking resources, global, regional and I/O clocking techniques, memory, FIFO resources, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the families (PCI Express® technology, analog to digital converters and gigabit transceivers) are also introduced.
This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

Level: FPGA3

Training Duration: 1 day

Who Should Attend?

For those who have taken the Essentials of FPGA Design course.

Prerequisites:

- Essentials of FPGA Design (introductory FPGA course)
- Intermediate VHDL or Verilog knowledge
- Introduction with the Virtex devices

What Should You Already Be Able to Do?

- However, time will not be spent now to review these items
  - Describe the basic Xilinx software flow
  - Describe the basic implementation options of the ISE tools
  - Describe global timing and I/O constraints

Software Tools:

ISE Design Suite 13.1

Hardware:

Artix-7, Kintex-7, and Virtex®-7 FPGAs
Demo board: None

Skills Gained: After completing this training, you will be able to:

- Describe all the functionality of the 6-input LUT and the CLB construction of the 7 series FPGAs
- Specify the CLB resources and the available slice configurations for the 7 series FPGAs
- Define the block RAM, FIFO, and DSP resources available for the 7 series FPGAs
- Properly design for the I/O block and SERDES resources in the 7 series FPGAs
- Identify the MMCM, PLL, and clock routing resources included with these families
- Identify the hard resources available for implementing high-performance DDR3 physical layer interfaces
- Describe the additional dedicated hardware for all the 7 series family members
- Properly code your HDL to get the most out of the 7 series FPGAs

Course Outline

1. 7 Series FPGA Overview

2. CLB Architecture
Lab 1: CLB Resources

3. I/O Resources
Lab 2: I/O Resources
4. Clocking Resources
Lab 3: Clocking Resources

5 Dedicated Hardware

10. Coding Techniques

11. 7 Series FPGA main changes Overview

Lab Description

Lab 1: CLB Resources –Using XST, synthesize a 32-bit incrementer with terminal count logic and pipelining registers. Verify that the appropriate resources were used with the RTL and technology viewers included with XST. Use the FPGA Editor to inspect the implemented results.
Lab 2: I/O Resources – Using the CORE Generator I/O Interface Wizard, construct a high-speed, clock-forwarded output interface. Explore through simulation the behavior of the various blocks. Also use the FPGA Editor to explore the physical resources of the 7 series FPGA tile used for construction of the high-speed output interface.

Lab 3: Clocking Resources – Using the Clocking Wizard, build and optimize the appropriate MMCM and clock routing resources. Also instantiate these resources into the design. After the design is implemented, verify hardware usage with the FPGA Editor and explore other aspects of the silicon layout.