Essentials of FPGA Design

Course Description

Build an effective FPGA design using synchronous design techniques, instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments, set basic XDC timing constraints, and use the Vivado™ Design Suite to build, synthesize, implement, and download a design.

Level: FPGA 2

Training Duration: 2 days

Who Should Attend?

Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites:

- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Other Optional RELs

- Basic HDL Coding Techniques
- Virtex-6 and Spartan-6 FPGA HDL Coding Techniques

Software Tools:

- Vivado System Edition 2012.4

Hardware:

- Architecture: 7 series FPGAs**
- Demo board: Kintex™-7 FPGA KC705 board**

Skills Gained: After completing this training, you will be able to:

- Take advantage of the primary 7 series FPGA architecture resources
- Use the Project Manager to start a new project
- Identify the available Vivado IDE design flows (project based and non-project batch)
- Identify file sets (HDL, XDC, simulation)
- Analyze designs by using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer
- Synthesize and implement an HDL design
- Utilize the available synthesis and implementation reports to analyze a design (utilization, timing, power, etc.)
- Build custom IP with the IP Library utility
- Make basic timing constraints (create_clock, set_input_delay, and set_output_delay)
- Use the primary Tcl-based reports (check_timing, report_clock_interaction, report_clock_networks, and report_timing_summary)
- Describe and analyze common STA reports
- Identify synchronous design techniques
- Describe how an FPGA is configured

Course Outline

1. Design Methodology Summary
2. Basic FPGA Architecture
3. Introduction to the Vivado Design Suite
4. Vivado Design Flows
Lab 1: Vivado Tool Overview
5. Visualization for Analysis
6. Designing with IP
7. Basic Timing Constraints and Reports
Lab 2: Vivado Synthesis and Implementation
8. Designing with FPGA Resources
9. Clocking Resources
Lab 3a: Designing with FPGA Resources
Lab 3b: Creating an IP Integrator Subsystem Design
10. Basic Timing Constraints (XDC)
11. Timing Reports
Lab 4: Basic XDC and Timing Reports
12. Synchronous Design Techniques
13. FPGA Configuration
Appendix: SystemVerilog
Appendix: Design Methodology
Appendix: HDL Coding Techniques
Appendix: Using the Pin Planning Environment

Lab Description

Lab 1: Vivado Tool Overview – Create a project in the Vivado Design Suite. Add files, simulate, and elaborate the design. Review the available reports, analyze the design with the Schematic and Hierarchy viewers, and run a design rule check (DRC). Finally, assign some of the I/O pins using the IO Planner.
Lab 2: Vivado Synthesis and Implementation – Vivado Synthesis and Implementation – Synthesize and analyze the design with the Schematic viewer, review XDC timing constraints, and run basic static timing analysis. Implement the design and analyze with the Schematic viewer. Download the bitstream.
Lab 3a: Designing with FPGA Resources – use the Xilinx Clocking Wizard to configure a clocking subsystem to provide various clock outputs and clock buffers to connect clock signals to global clock networks.
Lab 3b: Creating an IP Integrator Subsystem Design – Use the IP Integrator to create a complex system design by instantiating and interconnecting IPs from the Vivado IP Catalog on a design canvas.
Lab 4: Basic XDC and Timing Reports – Use timing constraints to improve design performance. Perform static timing analysis before and after implementation to validate the performance results.