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FPGA Power Optimization

Course Description

Attending the *FPGA Power Optimization* class will help you create a more power efficient FPGA design. This course can help you fit your design into a smaller FPGA, reduce your FPGA's power consumption, or run your FPGA at a lower temperature.
In addition, by mastering the tools and design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs.

Level: FPGA 2

Training Duration: 1 day

Who Should Attend?

FPGA designers with intermediate knowledge of HDL and some experience with the Xilinx Vivado® Design Suite tools

Prerequisites:

- Essentials of FPGA Design course or equivalent knowledge of FPGA architecture features; the Xilinx implementation software flow and implementation options; reading timing reports; basic FPGA design techniques; global timing constraints and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Recommended

- Designing for Performance course
- Basic FPGA Architecture: Memory and Clocking Resources

Software Tools:

- Vivado Design or System Edition 2014.3

Hardware:

- Architecture: 7 series FPGAs*
- Demo board: N/A*

Skills Gained: After completing this training, you will be able to:

- Use the Xilinx Power Estimator spreadsheet to estimate your design's power consumption after synthesis or implementation to build a better power estimate
- Use Power Report in the Vivado Design Suite to estimate your design's power consumption after implementation has been completed
- Import activity rates to complete a dynamic power estimation and build the most accurate power estimate
- Use the power_opt implementation options to automatically reduce your design's power consumption
- Use optimum HDL coding techniques and design practices to reduce your design's power consumption

Course Outline

1. Introduction

2. FPGA Power Requirements

3. Xilinx Power Estimator Spreadsheet (XPE)

4. Lab 1: Power Estimation with XPE

5. Vivado Power Analysis and Optimization

6. Lab 2: Power Analysis with the Vivado IDE

7. Lab 3: Dynamic Power Estimation with the Vivado IDE

8. Power Management Design Techniques

9. Power Optimization of I/O Resources

10. 7 Series Power Management Features

11. UltraScale Architecture Power Management Techniques

12. How to Solve a Power Problem

13. Worse-Case Thermal Calculations (optional)

14. Spartan-6 FPGA Power Management Features (optional)

15. Virtex-6 FPGA Power Management Features (optional)

16. Power and Temperature Measurement Features (optional)

17. Introduction to Partial Reconfiguration (optional)

Lab Description

Lab 1: Power Estimation with XPE – Estimate the resources required based on the high-level design description. Enter the amount of resources and default activity rates for the design and evaluate the estimated power calculated by XPE.
Lab 2: Power Analysis Using the Vivado IDE – Estimate the design's power consumption at synthesis and implementation with the Vivado power report. Generate a power report by using vectorless and vector-based mode and export the power report to the Power Estimator.
Lab 3: Dynamic Power Estimation with the Vivado IDE – Run the post-synthesis functional simulation of the design to generate a switching activity interchange format (SAIF) file. Create a power report with vectorless and vector-based activity information to verify the design's dynamic power consumption.