How to Design a High-Speed Memory Interface

Course Description

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debugging using 7 series FPGAs. Additionally, students will learn about the tools available for high-speed memory interface design, debug, and implementation of high-speed memory interfaces.

The major memory types covered are DDR2 and DDR3. The following memory types are covered on demand: RLDRAMII, LPDDR2, and QDRII+. Labs are available for DDR3 on the Kintex®-7 FPGA KC705 board.

Level: Connectivity 3

Training Duration: 2 days

Who Should Attend?

FPGA designers and logic designers

Prerequisites:

- VHDL or Verilog experience or Designing with VHDL or Designing with Verilog course
- Familiarity with logic design: state machines and synchronous design
- Very helpful to have:
    - Basic knowledge of FPGA architecture
    - Familiarity with Xilinx implementation tools
- Nice to have:
    - Familiarity with I/O basics
    - Familiarity with high-speed I/O standard

Software Tools:

- Vivado® System Edition 2015.1
- Mentor Graphics QuestaSim Advanced Simulator 10.3d
- Mentor Graphics HyperLynx SI 9.x

Hardware:

- Architecture: 7 series FPGAs*
- Demo board: Kintex-7 FPGA KC705 board*

Skills Gained: After completing this training, you will be able to:

- Identify the FPGA resources required for memory interfaces
- Describe different types of memories
- Utilize Xilinx tools to generate memory interface designs
- Simulate memory interfaces with the Xilinx Vivado simulator
- Implement memory interfaces
- Identify the board design options for the realization of memory interfaces
- Test and debug your memory interface design
- Run basic memory interface signal integrity simulations

Course Outline

1. **Course Introduction**
2. **7 Series FPGAs Overview**
3. **Memory Devices Overview**
4. **7 Series Memory Interface Resources**
5. **Memory Controller Details and Signals**
6. **MIG Design Generation**
7. **Lab 1:** MIG Core Generation
8. **MIG Design Simulation**
9. **Lab 2:** MIG Design Simulation
10. **MIG Design Implementation**
11. **Lab 3:** MIG Design Implementation
12. **Memory Interface Test and Debugging**
13. **Lab 4:** MIG Design Debugging
14. **MIG in Embedded Designs**
15. **Lab 5:** MIG in IP Integrator
16. **Memory Interface Board-Level Design**
17. **DDR3 PCB Simulation (optional)**
18. **Lab 6:** DDR3 Signal Integrity Simulation (optional

Lab Description

Lab 1: MIG Core Generation – Create a DDR3 memory controller using the Memory Interface Generator (MIG) in the Vivado IP catalog. Customize the soft core memory controller for the board.

Lab 2: MIG Design Simulation – Simulate the memory controller created in Lab 1 using the Vivado simulator or Mentor Graphics QuestaSim simulator.

Lab 3: MIG Design Implementation – Implement the memory controller created in the previous labs. Modify constraints, synthesize, implement, create the bitstream, program the FPGA, and check the functionality.

Lab 4: MIG Design Debugging – Debug the memory interface design utilizing the Vivado logic analzyer.

Lab 5: MIG in IP Integrator – Use the block design editor to include the MIG IP in a given processor design.

Lab 6: DDR3 Signal Integrity Analysis – Learn basic signal analysis options to check waveforms and design optimization (optional).