Tips and Tricks for FPGA Designers

Course Description

Attending the Tips & Tricks for FPGA Design class will enrich your knowledge in several aspects of the FPGA design world. This one day seminar will enable you to get familiar with new aspects and problems you may encounter during your project flow. In addition, by mastering the tools and the design methodologies presented in this course, you will be able to create your design faster, shorten your development time, lower the design risk and development costs.

Level: Intermediate

Training Duration: 1 day

Who Should Attend?

FPGA designers with intermediate knowledge, technical leaders and system engineers.

Prerequisites:

- Fundamentals of FPGA Design flow.
- Knowledge in FPGA design tools.
- Solid electrical design background

Software Tools:

ISE 13.1, PlanAhead, ChipScope, other useful utilities

Skills Gained: After completing this training, you will be able to:

- New methodologies
- New design rules
- Clock tree architecture
- Floorplanning techniques
- Use the advance implementation option
- Design your next project with better understanding and lower the risk

Course Outline

1. FPGA Designers – It is all about architecture?

2. Clock Tree Architecture

- Virtex6/Spartn6
- Virtex5
- Virtex4

Lab – Connecting High Speed DDR Parallel I/F in FPGA

3. ChipScope

- Basic Overview on ChipScope capabilities
- Tips & Tricks for ChipScope use

Lab - The power of ChipScope

4. Configuration – Partial Configuration

5. Advanced I/O Timing Constraints

- Purpose of timing constraints
- Differences between (SDR) and Double Data Rate (DDR) interfaces Use unique Pblock capability
- Analyze a timing report

6. Routing Optimization in Virtex-6 Devices

- Analyze the implementation results
- Design techniques that optimize routing

7. Reset effect on FPGA devices

- Implication of global reset
- The differences between synchronous versus asynchronous resets
- Local reset

For registration and details
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