

UltraFast Design Methodology

Course Description

This course describes the FPGA design best practices and skills to be successful using the Vivado® Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level: FPGA 3

Training Duration: 1 day

Who Should Attend?

Engineers who seek training for FPGA design best practices that increase design performance and increase development productivity.

Prerequisites:

- Some knowledge of FPGA design techniques is helpful
- Experience with the Vivado Design Suite or attendance of one of our existing Vivado Design Suite training courses is required
- Intermediate knowledge of Verilog or VHDL

Related Videos

- Vivado Design Methodology
- Vivado Design Flows Overview

Software Tools:

- Vivado Design or System Edition 2016.1

Hardware:

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board: None*

Skills Gained: After completing this training, you will be able to:

- Describe the *UltraFast Design Methodology Checklist*
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the UltraFast™ design methodology techniques work effectively through case studies and lab experience

Course Outline

1. UltraFast Design Methodology Case Study
2. Demo 1: UltraFast Design Methodology Checklist
3. UltraFast Design Methodology
4. HDL Coding Techniques
5. Resets
6. Lab 1: Resets
7. Inference
8. Lab 2: Inference
9. Synchronization Circuits
10. Demo 2: Synchronization Circuits
11. Baselineing
12. Demo 3: Baselineing
13. Timing Closure and Design Conversion Lab Introduction
14. Lab 3: Timing Closure and Design Conversion
15. Pipelining
16. Lab 4: Pipelining
17. Register Duplication
18. Physical Optimization
19. I/O Flip-Flops

Lab Description

Lab 1: Resets – Investigate the proper design and use of resets. Examine the impact of seeing a design built originally with asynchronous resets, having resets removed, and finally with synchronous resets only used where necessary.

Lab 2: Inference – Evaluate the implementation results of a design that uses asynchronous resets and infers more dedicated hardware resources when resets are selectively removed from the design. You will also learn how to infer the DSP hardware resources for other common functions required by most FPGA designs.

Lab 3: Timing Closure and Design Conversion – Learn how a generic processor design was optimized for the 7 series device architecture with basic design changes that impacted the dedicated hardware usage, design speed, and the device utilization.

Lab 4: Pipelining – Explore how pipelining can improve performance (increased clock rate and throughput) and facilitate timing closure.