

Vivado Design Suite Hands-on Introductory Workshop

Course Description

This course offers introductory training on the Vivado® Design Suite. This course is for experienced ISE® software users who want to take full advantage of the Vivado Design Suite feature set. Learn about the Vivado Design Suite projects, design flow, Xilinx Design Constraints, and basic timing reports.

Level: FPGA 1

Training Duration: 1 day

Who Should Attend?

Existing Xilinx ISE software Project Navigator FPGA designers

Prerequisites:

- FPGA design experience
- Completion of Essentials of FPGA Design or equivalent knowledge of the Xilinx ISE software implementation tools and device architecture

Software Tools:

- Vivado Design or System Edition 2013.3

Hardware:

- Architecture: 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board**

Skills Gained: After completing this training, you will be able to:

- Use the New Project wizard to create a new Vivado IDE project
- Describe the supported design flows of the Vivado IDE
- Generate a DRC report to detect and fix design issues early in the flow
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Explore synthesis and implementation options and directives
- Synthesize and implement the HDL design
- Use the "baselining" process to gain timing closure on the design
- Generate the various reports at synthesis and implementation by using the Tcl Console and Flow Navigator to analyze the design
- Use the Schematic and Hierarchy viewers to analyze and cross probe the design
- Use the Vivado IDE IP flow to customize IP and generate the output products
- Differentiate between the XCI and DCP files in the Vivado IDE IP flow
- Generate the various reports at synthesis and implementation by using the Tcl Console and Flow Navigator to analyze the design
- Use the Schematic and Hierarchy viewers to analyze and cross probe the design
- Use the Vivado IDE IP flow to customize IP and generate the output products
- Differentiate between the XCI and DCP files in the Vivado IDE IP flow

Course Outline

Vivado Synthesis and Implementation

Performance Baselining

Vivado Design Flows

Demo: Vivado IDE Overview

Lab 1: Vivado IDE Overview

Demo: Vivado DRC, Synthesis, and Implementation

Lab 2: Vivado Synthesis and Implementation

Lab 3: Vivado Design Rule Checker

Demo: Vivado Reports

Lab 4: Vivado Reports

Demo: Basic Design Analysis

Lab 5: Basic Design Analysis

Demo: Designing with the IP Integrator

Lab 6: Designing with IP

Lab Description

Lab 1: Vivado IDE Overview – Create a project by using the New Project wizard in the Vivado IDE. Add files to the project by using the Add Sources wizard. Explore the Project Manager and Flow Navigator and simulate the design. Review the options available in the Flow Navigator.

Lab 2: Vivado Synthesis and Implementation – Make timing constraints according to the design scenario. Modify synthesis and implementation settings. Synthesize and implement the design. Generate and download the bitstream to the demo board.

Lab 3: Vivado Design Rule Checker – Run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations.

Lab 4: Vivado Reports – Generate the Timing Summary report and Clock Networks report on the synthesized design. Review the contents of the Timing Summary, Utilization, and Check Timing reports after implementing the design.

Lab 5: Basic Design Analysis – Synthesize the design and use the Schematic and Hierarchy viewers to analyze the design. Implement the design and analyze some timing-critical paths with the Schematic viewer.

Lab 6: Designing with IP – Generate an IP from the Vivado IP catalog. Customize and generate the output products for the IP. Review the DCP and XCI files. Instantiate the IP in the design.