Zynq All Programmable SoC Accelerators

Course Description
Custom processor accelerators are quickly becoming standard practice for reaching system performance goals. This one-day introduction to the accelerator development flow focuses on how to measure system performance, determine what software functionality should be moved to hardware, how to assemble a custom accelerator using the Vivado® HLS tool, add the custom accelerator to a Zynq® All Programmable SoC design, and finally measure accelerated performance. Emphasis is placed on the Zynq AP SoC's architectural features that make coupling an accelerator to the multi-processor core a possibility as well as the many techniques for implementing accelerated systems. Discussion of typical tradeoffs that a system architect will likely make is also included. The specifics of the accelerator itself is secondary as the focus is on how to integrate an accelerator rather than accelerator design techniques.

Level: Embedded 2
Training Duration: 1 day

Who Should Attend?
System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC with hardware acceleration.

Prerequisites:
- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic understanding of system architecture

Software Tools:
- Vivado® Design or System Edition 2014.3
- Vivado HLS tool
- Xilinx SDK

Hardware:
- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

Skills Gained: After completing this training, you will be able to:
- Identify which system architecture best fits the design needs: data flow or accelerator
- Determine if software is meeting behavioral and performance specifications
- Profile an existing application to determine which functions are candidates for moving to hardware; design, from the ground up, an appropriately architected accelerator system
- Construct an accelerator using the Vivado HLS tool
- Assemble an embedded system using the Vivado IP integrator, including the custom accelerator
- Architect a memory system and memory access to best support an accelerator architecture
- Measure the performance of the complete system, including AXI loading

Course Outline
1. Introduction and Agenda
2. Zynq AP SoC Architecture Support for Accelerators
   Lab 1: Impact of Port Selection on System Performance
3. Accelerator Development Process
   Lab 2: Measuring Performance and Profiling
4. Coding Techniques for Accelerators
5. Developing the Accelerator Using HLS
   Lab 3: Building a Hardware Accelerator Using the Vivado HLS Tool
6. Building the Embedded Design Using IPI
   Lab 4: Building an Accelerated Embedded System (Accelerator Model)
7. Memory Concepts
   Measuring Embedded System Performance
   Lab 5: Measuring Accelerated System Performance

Lab Description
Lab 1: Impact of Port Selection on System Performance
   – The Zynq AP SoC has a number of ports. Connecting the accelerator to the wrong one could significantly hamper system performance. This lab explores the balance between loading the AXI ports and processor performance.

Lab 2: Measuring Performance and Profiling
   – Here you will learn how to measure system performance and determine through profiling which software functions should be moved to hardware in the form of an accelerator.

Lab 3: Building a Hardware Accelerator Using the Vivado HLS Tool
   – The Vivado HLS tool is a powerful C/C++ to netlist building tool that greatly facilitates converting software functions to hardware accelerators.

Lab 4: Building an Accelerated Embedded System (Accelerator Model)
   – This lab explores how the accelerator can be attached to the PS.

Lab 5: Measuring Accelerated System Performance
   – Having completed a full build of the accelerated embedded system, you will now confirm proper behavior and overall system performance.