Zynq All Programmable SoC System Architecture

Course Description
The Xilinx Zynq® All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course provides experienced system architects with the knowledge to effectively architect a Zynq All Programmable SoC. This course presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC.

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level: Embedded Software 3

Training Duration: 3 days

Who Should Attend?
System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC.

Prerequisites:
- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools:
- Vivado® Design or System Edition 2016.1

Hardware:
- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

Skills Gained: After completing this training, you will be able to:
- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline
1. Zynq All Programmable SoC Overview
2. Inside the Application Processor Unit (APU)
3. Lab 1: Building a Zynq All Programmable SoC Platform
4. Processor Input/Output Peripherals
5. Introduction to AXI
6. Zynq All Programmable SoC PS-PL Interfaces
7. Lab 2: Integrating Programmable Logic on the Zynq All Programmable SoC
8. Lab 3: Using DMA on the Zynq All Programmable SoC
9. Zynq All Programmable SoC Memory Resources
10. Meeting Performance Goals
11. Lab 4: Impact of Port Selection on System Performance
12. Zynq All Programmable SoC Design
13. Debugging the Zynq All Programmable SoC
14. Lab 5: Debugging on the All Programmable SoC Tools and Reference Designs
15. Lab 6: Running and Debugging a Linux Application on the Zynq All Programmable SoC

Lab Description
Lab 1: Building a Zynq All Programmable SoC Platform
Examine the process of using the Vivado IP Integrator tool to create a simple processing system.

Lab 2: Integrating Programmable Logic on the Zynq All Programmable SoC
Connect a programmable logic (PL) design to the embedded processing system (PS).

Lab 3: Using DMA on the Zynq All Programmable SoC
Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.

Lab 4: Impact of Port Selection on System Performance
Explore bandwidth issues surrounding the use of the Accelerator Coherency Port (ACP) and the High Performance (HP) ports.

Lab 5: Debugging on the All Programmable SoC
Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.

Lab 6: Running and Debugging a Linux Application on the Zynq All Programmable SoC
Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.