Zynq Board Design and High-Speed Interfacing

Course Description

Are you interested in learning how to effectively utilize Zynq-7000 SoC high-speed interface resources? This course supports both experienced and less experienced designers who have in minimum general digital hardware knowledge and basic information on Zynq devices. Furthermore, first work with the new Xilinx VIVADO Design Suite is helpful. This course focuses on understanding as well as how to properly design for the high-speed interface solutions found in the new device families: transceiver in general, PCI Express and memory interfacing complemented with board design issues. Topics covered include interface overviews, design usage, simulation, implementation and examples on real hardware.
This course also includes a detailed discussion about proper PCB design techniques that enables designers to avoid common mistakes and get the most out of their FPGA interfaces.
A combination of modules and labs allow for practical hands-on application of the principles taught.

Training Duration: 2 days

Who Should Attend?

- Xilinx hardware designers

Prerequisites:

- Essentials of FPGA Design course
- Intermediate VHDL or Verilog knowledge Software Tools: ISE Design Suite 14.x

Software Tools:

- VIVADO Design Suite 2013.3

Hardware:

- ZYNQ-7000
- Demo board: ZC706 / (KC705)

Skills Gained: After completing this training, you will be able to:

- Describe the functionality of transceivers, PCIe blocks and memory interfaces
- Configure the corresponding wizards to design high-speed interfaces
- Simulate and implement high-speed interfaces
- Start practical work with high-speed interfaces
- Describe challenges and solutions for successful powering and interfacing high-speed interfaces on PCB level
- Apply high-speed interface specific signal integrity rules in PCB design

Course Outline

1. Introduction to high-speed connectivity

2. Zynq Board Design

- General design constraints
- Signal integrity on chip level (IO region)
- Power options, requirements and solutions
- Power estimation in XPE vs. Power calculations in Vivado
- Powering transceivers - requirements and solutions
- Powering memory interfaces - requirements and solutions
- Board design for Agile Mixed Signal
- Signal integrity on board level
- Board design checklist

3. Serial transceiver

- Transceiver overview (7 series FPGAs and Zynq 7000)
- Basic principles and solutions in serial transmission
- Transceiver design

Lab1: Generating transceiver design

- Simulation and implementing transceiver interfaces
- Lab2: Transceiver simulation and implementation
- Debugging transceiver interfaces

Lab3: IBERT

4. PCI Express

- PCIe Basics
- Xilinx PCIe solutions
- PCIe endpoint design

Lab1: Generating PCIe endpoint

- Simulation and Implementation PCIe interfaces

Lab2: PCIe endpoint simulation and implementation

- Usage of PCIe endpoint in application

Lab3: PCIe endpoint in real system with ZC706 / (KC-705) board

5. Memory Interfaces

- Memory devices overview
- Xilinx memory interface solutions
- DDR3 design

Lab1: Generating DDR3 controller

- Simulation and implementation memory interfaces

Lab2: DDR3 interface simulation and implementation

- Implementing memory interfaces

Lab3: Verification DDR3 interface on real hardware