Designing FPGAs Using the Vivado Design Suite 2

Course Description

You will learn to build an effective FPGA design, utilizing the Vivado® IP integrator to create a sub-system, employing proper HDL coding techniques to improve design performance, Performing pin assignments, Applying basic timing constraints, Illustrating the advanced capabilities of the Vivado® logic analyzer to debug a design, Identifying advanced FPGA configurations, Debugging a design at the device startup phase

Level: FPGA 2

Training Duration: 4 days

Who Should Attend? – Digital designers who have a knowledge of HDL (VHDL or Verilog).

Prerequisites:

- Basic HDL knowledge (Verilog or VHDL)
- Digital design knowledge and experience (attendees should be electrical engineers)

Software Tools:

- Vivado® Design Suite 2021.1

Skills Gained: **After completing this training, you will have the necessary skills to:**

- Create a Tcl script to create a project, add sources, and implement a design
- Describe and use the clock resources in a design
- Create and package your own IP and add to the Vivado IP catalog to reuse
- Use the Vivado IP integrator to create a block design
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Use the Xilinx Power Estimator (XPE) and Power Design Manager (PDM) tools
  Use the Schematic and Hierarchy viewers to analyze and cross-probe a design
  Use the Vivado logic analyzer and debug cores to debug a design
- Describe the Versal ACAP clocking architecture and hardware platform development using Vivado IP integrator
- Describe how power analysis and optimization is performed
- Describe the HDL instantiation flow of the Vivado logic analyzer
- Optimize HDL code to maximize the FPGA resources that are inferred and meet performance goals
- Describe how to enable remote debug
- Identify advanced FPGA configurations, such as daisy chains and gangs, for configuring multiple FPGAs in a design
- Debug a design at the device startup phase to debug issues related to startup events, such as MMCM lock and design coming out of reset

Course Outline:

1. **Introduction to FPGAs**
   Provides an overview of FPGA architecture and describes the advantages, applications, and major building blocks of FPGAs.
2. **Vivado Design Suite Project-Based Mode**
   Introduces project-based mode in the Vivado Design Suite, including creating a project, adding files to a project, exploring the Vivado IDE, and simulating a design
3. **Vivado IP Flow**.
   Demonstrates how to customize IP, instantiate IP, and verify the hierarchy of your design IP
4. **Basic Design Analysis in the Vivado IDE**
   Outlines the various design analysis features in the Vivado Design Suite
5. **Introduction to Clock Constraints**
   Shows how to apply clock constraints and perform timing analysis

6. **Timing Constraints Wizard**
   Reviews how use the Timing Constraints Wizard to apply missing timing constraints in a design
7. **Vivado Design Suite I/O Pin Planning**
   Describes the I/O Pin Planning layout for performing pin assignments in a design
8. **Power Estimation Using XPE**
   Illustrates estimating the amount of resources and default activity rates for a design and evaluating the estimated power calculated by XPE
9. **Power Analysis and Optimization Using the Vivado Design Suite**
   Illustrates using report power commands to estimate power consumption
10. **Dynamic Power Estimation Using Vivado Report Power**
    Use a SAIF (switching activity interface format) file to determine accurate power consumption for a design
11. **Power Management Techniques**
    Identify techniques used for low power design
12. **Introduction to FPGA Configuration**
    Describes how FPGAs can be configured.
13. **Configuration Process**
    Reviews the FPGA configuration process, such as device power up and CRC checks.
14. **Configuration Modes**
    Understand various configuration modes and select the suitable mode for a design.
15. **Daisy Chains and Gangs in Configuration**
    Introduces advanced configuration schemes for multiple FPGAs
16. **Bitstream Security**
    Understand the AMD Xilinx bitstream security features such as readback disable, bitstream encryption, and authentication
17. **Introduction to the Vivado Logic Analyzer**
    Provides an overview of the Vivado logic analyzer for debugging a design.
18. **Introduction to Triggering**
    Introduces the trigger capabilities of the Vivado logic analyzer.
19. **Debug Cores**
    Describes how the debug hub core is used to connect debug cores in a design.
20. **HDL Instantiation Debug Probing Flow**.
    Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer
21. **Netlist Insertion Debug Probing Flow**
    Covers the netlist insertion flow of the debug using the Vivado logic analyzer
22. **JTAG to AXI Master Core**
    Use this debug core to write/read data to/from a peripheral connected to an AXI interface in a system that is running in hardware.
23. **Debug Flow in an IP Integrator Block Design**
    Insert the debug cores into IP integrator block designs.
24. **Remote Debugging Using the Vivado Logic Analyzer**

Use trigger state machine code to trigger the ILA and capture data in the Vivado logic analyzer

25. **Vivado Design Suite Debug Methodology**
    Understand and follow the debug core recommendations. Employ the debug methodology for debugging a design using the Vivado logic analyzer.
26. **Trigger and Debug at Device Startup**
    Debug the events around the device startup.
27. **Trigger Using the Trigger State Machine in the Vivado Logic Analyzer**
    Use trigger state machine code to trigger the ILA and capture data in the Vivado logic analyzer
28. **Clock Structure and Layout in the UltraScale Architecture**
    Describes UltraScale clocking architecture and differences in the clocking architectures between 7 series and UltraScale FPGAs
29. **Clock Buffers in the UltraScale Architecture**
    Reviews the different clock buffers and clock migration.
30. **Clock Management in the UltraScale Architecture**
    Highlights clock management resources.
31. **Clock Routing in the UltraScale Architecture**
    Describes clock routing, distribution, and the benefits of clock routing
32. **UltraScale Architecture I/O Resources: Overview**
    Provides an overview of the I/O resources and I/O banks available the UltraScale architecture.
33. **UltraScale Architecture I/O Resources: Component Mode▪**
    Describes component mode, SelectIO™ interface logic, SERDES technology, and programmable delay lines.
34. **UltraScale Architecture I/O Resources: Native Mode**
    Describes SelectIO interface logic, BITSLICE technology, native mode clocking, and the High Speed SelectIO Wizard.
35. **Designing with the IP Integrator**
    Demonstrates how to use the Vivado IP integrator to create the uart_led subsystem
36. **Block Design Containers in the Vivado IP Integrator**
    Describes the block design container (BDC) feature and shows how to create a BDC in the IP integrator.
37. **Creating and Packaging Custom IP**
    Covers creating your own IP and package and including it in the Vivado IP catalog
38. **Using an IP Container**
    Illustrates how to use a core container file as a single file representation for an IP.
39. **Versal ACAP: Clocking Architecture**
    Discusses the clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skew in the Versal ACAP.

40. **Inference**
    Infer AMD Xilinx dedicated hardware resources by writing appropriate HDL code
41. **Sampling and Capturing Data in Multiple Clock Domains**
    Overview of debugging a design with multiple clock domains that require multiple ILAs
42. **Revision Control Systems in the Vivado Design Suite**
    Use version control systems with Vivado design flows.