Designing with PCI Express Gen 1.x – 4.0

Course Description

The course provides a detailed and comprehensive understanding of the PCI Express technology.

The course is fully up-to-date and supports the basic and latest version of the international specification (1.x - 4.0) and covers all aspects of the specification (software and hardware) and all other information which requires to design and integration of systems which includes PCI Express implementations.

This course provides example implementations, and practical guidance that will give a running start on your design.

Training Duration: 4 days

Who Should Attend? – This in-depth course is hardware and software oriented. It describes all options and performance, and as a result it is useful for hardware & software engineers and System Architecture as well.

Skills Gained: **After completing this training, you will have the necessary skills to:**

- The participants will be able to specify performance, define architecture, writing drivers, design hardware and system integration.

Course Outline:

Day 1

Chapter 1 - Legacy PCI – Fundamentals (Plug & Play)

- Performance
- Basic architecture
- Memory, I/O, and Configuration space
- Configuration process
- Data transfer
- PCI to PCI Transparent Bridge concept
- Posted & Non-Posted R/W

Chapter 2 – Introduction to PCI Express

- Why new I/O architecture
- Link and Lane definition
- Root Complex, Switch & Endpoint definition
- Layers overview (Transaction, Data & Physical)
- Card specification (Electrical and Mechanical)
- Advanced Switching (advanced peer to peer communication)

Chapter 3 – Mechanical Specification

- Connector types
- Add In Card form factor

Chapter 4 - Physical Layer

- Electrical Sub Block
- Card Specification
- Design guidelines
- Lanes
- Link State machine
- Link Training process
- Configuration space – Link Capability

Chapter 5 – Data Link Layer Basics

- Packet Types
- Packet Format
- Data Link Layer Packet (DLLP)
- Timeout
- Retry
- TLP Header Format
- Request Rules
- Completion Rules
- Maximum Packet Size

Chapter 6 – Transaction Layer –

- Layering Overview
- Transaction Types (Memory, I/O, Configuration, Messages)

Day 2

Chapter 7 – System Architecture

- ECRC
- Message Type
- Error Signaling
- Flow Control
- Quality of Service (QoS)
- Cut-Through
- Interrupt Mechanism
  - INTx,
  - MSI
  - MSI-X
- Intel x86 Chipset

Day 3

Chapter 8 – Power

- Reset
- Power Management (PM)
- Clocks & Clock Request (CLKREQ#)
- Slot Capability
- Hot Plug – basics
- Hot Plug/ Removal implementation

Chapter 9 - Configuration Space

- Type 0 Configuration Space
- PCIe Capability Structure (inside legacy configuration space)
    - PCI Express Capabilities
    - Device Capabilities
    - Link Capabilities
    - Slot Capabilities
    - Root Complex
- Extended capabilities
    - Advanced Error Reporting
    - Virtual Channel

Chapter 10 – Examples

- Switch Datasheet
- Throughput
- Configuration Space
    - ECAM
    - Analysis of NVIDIA Video
- board configuration Space

Chapter 11 – Introduction to PCIe Gen 3 & 4

Day 4 – PCIe Gen 3.x & Gen 4.0

Chapter 12 – Physical Layer

- 8GT/s & 16GT/s Encoding
- 8GT/s & 16GT/s Link Equalization
- Link Initialization & Training
- LTSSM
- Configuration Space
- Lane Margining at Receiver
- PCIe Compliance

Chapter 13 – Power Management & Retimers

- L1 Sub States (L1.0, L1.1, L1.2)
- Emergency Power Reduction (PWRBRK)
- Retimers

Chapter 14 – Gen 3 New Features

- Multicast Operation
- Atomic Operation
- Dynamic Power Allocation
- Latency Tolerance Reporting (LTR)

Chapter 15 – I/O Virtualization & Sharing (SR-IOV)

- Architecture Overview
- Interoperability
- Reset
- Re-Initialization & Resource Allocation
- Virtual Function (VF)
- Configuration Space
- Interrupts
- Power Management
- ATS

Appendix 1: PCIe Over Cable

Appendix 2: Add_in_card checklist