

Signal Integrity and Board Design Using HyperLynx

Course Description

Learn when and how to apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and other components. This comprehensive course combines design techniques and methodology with relevant background concepts of high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS & IBIS AMI models and complete simulations using Mentor Graphics HyperLynx. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules with instructor demonstrations and practical hands-on labs.

Level: Connectivity 3

Course Part Number: CONN-SI

Training Duration: 4 days

Who Should Attend? – Digital designers, board layout designers, or scientists, engineers, and technologists seeking to implement Xilinx solutions. Also end users of Xilinx products who want to understand how to implement high-speed interfaces without incurring the signal integrity problems related to timing, crosstalk, and overshoot or undershoot infraction

Prerequisites:

- FPGA design experience preferred (Designing FPGAs Using the Vivado Design Suite 1 course or equivalent)
- Familiarity with high-speed PCB concepts
- Basic knowledge of digital and analog circuit design
- Basic experience in handling of new software tool
- Vivado™ tool knowledge is helpful
- Hyperlynx tool knowledge is helpful

Software Tools:

- Mentor Graphics HyperLynx 8.2.1

Hardware

- Architecture: N/A*
 - Demo board: None*
- * This course does not focus on any particular architecture

Skills Gained: After completing this training, you will have the necessary skills to:

- Describe signal integrity effects
- Predict and overcome signal integrity challenges
- Simulate signal integrity effects
- Verify and derive High-Speed design rules for the board design
- Apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and semiconductor circuits
- Understand S-parameters and simulate with IBIS-AMI
- Plan your board design under FPGA-specific restrictions
- Supply the FPGAs with power
- Handle thermal aspects
- Simulate signal integrity effects using IBIS- & IBIS-AMI models at High Multi-Gigabit rates
- Understand Serial transceivers usage with both TX & RX equalization signal impairments including Hands-on tips
- Design Multi-Gigabit high speed links through high frequency design flow: S-parameters, Pre-Layout and Post-Layout Simulations
- Understand High speed links from Analog/RF point of view
- Debug High-Speed Multi-Gigabit links via High frequency techniques such as multi-mode S-parameters

Course Outline:

Signal Integrity

- Signal Integrity Introduction
- Transmission Lines
- IBIS Models and SI Tools
- **Lab 1:** Invoking HyperLynx
- Reflections
- **Lab 2:** Reflection Analysis
- Crosstalk
- **Lab 3:** Crosstalk Analysis
- FPGA Power Supply
- Power Supply Issues
- Signal Interfacing: Interfacing in General
- **Lab 4:** DDR3/4 Example
- PCB Details & Die Architecture and Packaging
- Thermal Aspects
- FPGA Configuration and PCB
- Signal Interfacing: FPGA-Specific Interfacing
- **Lab 5:** Case study
- High-Speed SerDes Transceivers Overview
- Introduction to S-parameters for High-Speed applications
- Introduction to IBIS-AMI models & High-Speed hands-on design tips
- **Lab 6:** Pre-layout simulation with IBIS-AMI models (~25Gbps)
- **Lab 7:** Post-layout simulation with IBIS-AMI models (~25Gbps)
- Course Summary

Lab Description

- **Lab 1:** Invoking HyperLynx – Become familiar with signal integrity tools. Use HyperLynx for schematic entry, modeling, and simulation. Modify a standard IBIS model to define a driver and then use its stackup editor to define a PCB.
- **Lab 2:** Reflection Analysis – Define a circuit and run various simulations for effects of reflection.
- **Lab 3:** Crosstalk Analysis – Using simulation, analyze circuit topology and PCB data for strategies to minimize crosstalk.
- **Lab 4:** DDR3/4 – Simulate DDR design including eye diagram.
- **Lab 5:** Case study – whiteboard exercised on SI effects.
- **Lab 6:** Pre-layout simulation with IBIS-AMI models.
- **Lab 7:** Post-layout simulation with IBIS-AMI models.